High Speed VLSI Simulator
Qi Chen, Pan Zhang. Supervisor: Prof. Sourajeet Roy
Department of Computer and Electrical Engineering
Colorado State University

Background

Interconnects
- transmission lines, copper wires, and Carbon nano-tubes
- Board to board, chip to chip, PCB, on chip level

High-speed
- High frequency clock rates
- Short signal rise-time

Current Challenges
- The lack of efficient methods of characterizing interconnects. No exact time domain solution exists, and is currently done by discretizing PDE to approximate to its ODE representation.
- Distributed element, tradeoffs between CPU cost and accuracy

Objectives

Fall Semester
- Design and develop a general purpose circuit simulator capable of CAD of high-speed interconnect
- Frequency domain and time domain simulation
- Single conductor and multi conductor simulation

Spring Semester
- Reduce computation cost by investigating Model Order Reduction (MOR) method
- Reduces the number of unknowns to significantly decrease computation time

Methods

Tools
- Programs written in C++ and operates on CSU’s CRAY supercomputer
- Usage of an industry standard, HSPICE, as a result reference

Mathematical Models
- Modified Nodal Analysis
- ODE circuit representation and solution
- PDE representation of transmission lines

Technical Performance Measurements
- Accuracy
- CPU time
- Stability of the simulation results

Frequency Domain Analysis

Mathematical representation
- Layout to “Stamp” (MNA/ODE model)
- Laplace domain
- LU decomposition to solve the equation
  \( Gx + zC \dot{x} = B \)
  \( s = j2\pi f \)

Time Domain Analysis

Mathematical representation
- Using existing models from frequency domain analysis
- Using implicit numerical integration methods to approximate time domain solution
  - Backwards Euler method

Coupled Interconnect Simulation

The coupled multi-conductor circuits are analyzed and simulated in the time domain using the lumped model which is derived from Telegrapher’s partial differential equation with inductive and capacitive coupled effects, and solved using Backward Euler. This part of the solver is tested using the following test module. The coupled voltage is shown below.

Model Order Reduction

Model order reduction method essentially reduces the number of unknowns such as the node voltages and branch currents. This method is used to significantly decrease computation time for both time and frequency domain analysis. It utilizes the projection of matrix onto its Krylov Subspace and finding its orthogonalized matrix Q with reduced number of columns. In this case, we chose the reduced number of columns to be 400 for both the frequency and time domain analysis of the 6 conductor testing module. The reduced CPU cost is shown above.

Conclusion

The objective of developing a general VLSI circuit simulator with ability to perform CAD of high-speed interconnects and optional model order reduction capability have been completed successfully. This will become a continuation project for future senior design teams to implement non-linear circuit simulation and parallel computation.

References